

Hardware Errata

This page lists some issues with the hardware.

Rev 2

- Holes for current sense resistors should be slightly larger
 - Datasheet specifies $1.5\text{mm} \pm 0.12\text{mm}$
- Increase spacing between heatsink and MOSFET/resistor slightly
 - Right now, the legs need to be bent at a bit of an angle, which makes fitting everything a huge pain in the ass
- Zero offset resistor (R307, ???) is too large
 - 4M7 is too large and doesn't let us trim out the entire DC offset ($\sim 4.5\text{mV}$)
 - 1M was also too large ($\sim 3.5\text{mV}$)
 - 200k works (able to trim to $\sim 1\mu\text{V}$ remaining offset)
 - This is probably too low, maybe something like 330k or 500k is better
 - The trimming range is quite small

Rev 1

- MOSFET gate drive voltage too low
 - V_{Gs} , with the current configuration can only drive to max +3V3. This is not sufficient to turn on the MOSFETs selected (IXTH80N075L2) with a $V_{\text{Gs}}(\text{th})$ of 4.5V max
 - May be salvageable by rework (op-amp powered from 5V instead) and selecting a different MOSFET
 - Future work
 - Select a MOSFET driver opamp that can be powered from $\pm 12\text{V}$
 - Update power section to generate isolated 12V (replace PS201 with PDSE1-S12-S12-S)
 - Generate 5V locally (switching supply off 12V)
- I²C isolator (U203, ADuM1250) has the output SCL/SDA swapped
 - The I²C bus is swapped for all devices downstream of the EEPROM

Revision #5

Created 1 April 2022 18:55:49

Updated 29 May 2022 04:29:55