DMA Channel Allocations

DMAC should operate with dynamic, round-robin priority arbitration within a DMA priority level. Priority levels listed are from 0 (highest) to 3 (lowest.)

- Ch0: NOR flash SPI Tx empty (SERCOM5)
  - Priority: 2
  - Operate in SPI 32 bit data mode
  - Burst transfers
- Ch1: NOR flash SPI Rx complete (SERCOM5)
  - Priority: 2
  - Operate in SPI 32 bit data mode
  - Burst transfers
- Ch2: Display SPI Tx empty (SERCOM4)
  - Priority: 1
  - Operate in SPI 32 bit data mode
  - Burst transfers

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