Clocking

Clock Inputs

All clocks on the system are derived from one of the following clock inputs (oscillators and internal generators:)

Crystals

- XOSC1: External 12MHz oscillator
  - Provides primary system clock reference
- XOSC32K: External 32.768kHz oscillator
  - Runs in standby for RTC

FLLs

- DFLL48M: 48MHz
  - Used for USB reference clk
  - Uses external 32kHz osc for reference

PLLs

- DPLL0: 120MHz
  - CPU core clock

Clock Sources

The above clock inputs are then synthesized into multiple clock sources, each used by a different set of peripherals:

- GCLK0: 120MHz
  - Sourced from DPLL0 / 1
  - General high speed clock
- GCLK1: 48MHz
  - Sourced from DFLL48M
  - Intended for USB use
- GCLK3: 32.768kHz
  - Sourced from XOSC32K

- SERCOM slow clock
  - GCLK4: 12MHz
    - Sourced from XOSC1
    - General low speed clock
  - GCLK5: 32.768kHz
    - Sourced from ultra low power 32kHz osc

Clock Consumers

  - CPU core: GCLK0
    - Clock division factor: /1
    - Low power clock: /4
    - Backup domain: /8
    - High-speed: /1