

# Expansion

Peripherals can be connected to the CPU board through the expansion connector, a 96-pin, 3 row DIN41612 right angle connector.

## Pinout

	A	B	C
1	+5V	GND	+12V
2	+5V	GND	+12V
3	I2C_SCL <sup>1</sup>	/I2C_IRQ <sup>1</sup>	I2C_SDA <sup>1</sup>
4	GND	GND	GND
5	GND	D8	D13
6	D9	D11	D15
7	D10	D14	D12
8	D7	D5	GND
9	D6	GND	D3
10	GND	D4	D1
11	D2	D0	GND
12	GND	GND	A22
13	A23	GND	A19
14	GND	A21	A17
15	A20	A15	A18
16	A13	A16	A12

<b>17</b>	A14	A10	GND
<b>18</b>	A11	GND	A8
<b>19</b>	GND	A9	A6
<b>20</b>	A7	A4	A2
<b>21</b>	A5	A3	A1
<b>22</b>	R/W	/LDS	/UDS
<b>23</b>	GND	/DTACK <sup>1</sup>	/AS <sup>1</sup>
<b>24</b>	CLK	GND	
<b>25</b>	FC1	FC0	FC2
<b>26</b>			
<b>27</b>			/EXTRST <sup>1</sup>
<b>28</b>	/EXT <sup>5</sup>	/BG <sup>1</sup>	/HALT <sup>14</sup>
<b>29</b>	/RESET <sup>34</sup>	/BR <sup>1</sup>	/BGACK <sup>1</sup>
<b>30</b>	/IACK <sup>1</sup>	/IRQ	/BERR <sup>14</sup>
<b>31</b>	GND	GND	GND
<b>32</b>	SNDR	GND	SNDL

Note that the data and address bus, as well as most control signals (those in rows 1-25) should be driven through buffers when multiple peripherals are present. These buffers should be direction controlled by the bus request lines, as to allow external bus masters to access CPU board peripherals.

Any empty cells are not currently used and considered reserved for future use, and should be no connect.

## Remarks

1. Pulled up on CPU board
2. Pulled down on CPU board
3. Asserted by processor to reset all peripherals. To reset the processor, you must simultaneously assert /RESET and /HALT for at least 1ms.
4. This signal is open drain.

5. Asserted when the currently decoded address is valid *and* is not decoded on the CPU board. Can be used as part of external buffer logic.
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