Backplane

Cards are interconnected via a simple backplane. Together with a management card, the backplane provides power, bus control signals, out of band signaling and support for per card audio outputs.

- Pinout
- 6 Slot Backplane

Pinout

Using 96 position (3x32) DIN 41612 connectors; right angle male on expansion cards, vertical female on the backplane side. The management card uses a 48 position (3x16) DIN 41612 (C2) right angle male connector, with the corresponding vertical female on the backplane side.

CPU Board

The pinout of the CPU board's expansion connector is documented on the CPU board expansion page.

Management Card

This provides power input to the rest of the backplane, and provides connectors for the mixed audio from the backplane.

	A	B	C
1	+5V	+5V	+5V
2	+5V	+5V	+5V
3	+5V	+5V	+5V
4	GND	GND	GND
5	+12V	+12V	+12V
6	GND	GND	GND
7		GND	
8		GND	
9		GND	
10		GND	

11		GND	
12	/EXTRST	GND	
13		GND	I2C_IRQ
14	I2C_SCL	GND	I2C_SDA
15		GND	
16	SNDR	GND	SNDL

Any empty cells are not filled in are considered reserved for future use, and should be left unconnected.

Remarks

1. SNDL/SNDR refers to mixed audio from all cards (CPU + expansion) in the system.
2. EXTRST: when asserted, the CPU board (and with it, all peripherals on the backplane) are reset. This is equivalent to pushing the reset button on the CPU board, if it has one.

Peripheral

These connectors are provided by peripherals; they're 96-position, 3 row type C DIN 41612 connectors. They shall be right angle, male type.

	A	**B**	**C**
1	+5V	GND	+12V
2	+5V	GND	+12V
3	I2C_SCL[1]	/I2C_IRQ[1]	I2C_SDA[1]
4	GND	GND	GND
5	GND	D8	D13
6	D9	D11	D15
7	D10	D14	D12

8	D7	D5	GND
9	D6	GND	D3
10	GND	D4	D1
11	D2	D0	GND
12	GND	GND	A22
13	A23	GND	A19
14	GND	A21	A17
15	A20	A15	A18
16	A13	A16	A12
17	A14	A10	GND
18	A11	GND	A8
19	GND	A9	A6
20	A7	A4	A2
21	A5	A3	A1
22	R/W	/LDS	/UDS
23	GND	/DTACK	/AS
24	CLK	GND	
25	FC1	FC0	FC2
26			
27	/IRQ_IN	/DETECT	GND
28	/IRQ_OUT	/BG	/HALT[2]
29	/RESET[2]	/BR[2]	/BGACK[2]
30	/IACK	/IRQ[2]	/BERR[2]

31	GND	GND	GND
32	SNDR	GND	SNDL

Remarks

1. Pulled up to +5V by backplane
2. These signals should be driven as open drain; they're pulled up by either the backplane or CPU board.
3. If the card doesn't provide sound, tie SNDL/SNDR to ground through a 100kΩ resistor.
4. Cards should tie /DETECT to GND so that the backplane can detect which slots are occupied, even if the card doesn't have anything on its I^2C bus.

Interrupt Arbitration

Peripheral cards arbitrate interrupt priority in slot order. This works by means of a daisy-chained interrupt request line from each slot to the next. The first slot has the daisy chain input tied permanently high. Each peripheral outputs whether it has a pending interrupt on these pins, and then asserts the shared interrupt line. When an interrupt acknowledge cycle takes place, the peripheral with the highest priority – that is, whichever has an `/IRQ_IN` that's deasserted – responds.

When its interrupt conditions are cleared (from within its ISR,) it will deassert `/IRQ_OUT` and `/IRQ`. If there's a lower priority card requiring attention, the interrupt will fire again and it will respond. Otherwise, the processor returns to normal execution.

The `/IRQ_IN` pin on cards is pulled down to GND with a 1MΩ resistor on the backplane for all slots to prevent erroneous interrupt behavior if cards aren't inserted one after another in the backplane, e.g. the interrupt priority chain is broken. Cards can drive these pins either directly, or open drain, but in the latter case, it must provide the required pull up resistors. For open drain driving, a pull up value of at least 47kΩ is suggested.

6 Slot Backplane

A backplane which supports up to six expansion cards, meant to go into a 3U VME crate.

image-1643962680396.png

Features

- Direction-controlled buffers for address and data bus
- Mixer for audio from CPU board and expansion slots
- Detection of installed peripheral cards via detect lines
- An I^2C bus switch to allow CPU board independent access to each slot’s sideband bus
- Extremely low jitter clock distribution

It’s intended to be used in conjunction with the backplane management card for power, but the required +5V and +12V rails can also be provided through a 3.81mm pitch pluggable terminal block instead.

Assembly Notes

Here are some notes about hardware revisions.

Rev 1

- The ID EEPROM is an AT24CS16, which has a different protocol than the AT24CS32 specified in the schematic. The address pins are also "NC" there
- Drop resistors for orange/yellow LEDs (R401, R107, R108) should be a lower value
  - R401 probably got assembled wrong
- Drop resistors for yellow LEDs (R101, R102) should be slightly higher
  - Or, we just spec shittier green LEDs
  - They're just slightly too bright