68000 CPU Board

The standard 68komputer processor board, featuring 1MB of 0 wait state SRAM and flash, 32K of NVRAM + RTC, a 68681 DUART, I2C controller, and dual SAA1099 PSG’s.

- Expansion
- Rev1 Assembly Notes

Expansion

Peripherals can be connected to the CPU board through the expansion connector, a 96-pin, 3 row DIN41612 right angle connector.

Pinout

	A	B	C
1	+5V	GND	+12V
2	+5V	GND	+12V
3	I2C_SCL[1]	/I2C_IRQ[1]	I2C_SDA[1]
4	GND	GND	GND
5	GND	D8	D13
6	D9	D11	D15
7	D10	D14	D12
8	D7	D5	GND
9	D6	GND	D3
10	GND	D4	D1
11	D2	D0	GND
12	GND	GND	A22
13	A23	GND	A19
14	GND	A21	A17
15	A20	A15	A18
16	A13	A16	A12

17	A14	A10	GND
18	A11	GND	A8
19	GND	A9	A6
20	A7	A4	A2
21	A5	A3	A1
22	R/W	/LDS	/UDS
23	GND	/DTACK[1]	/AS[1]
24	CLK	GND	
25	FC1	FC0	FC2
26			
27			/EXTRST[1]
28	/EXT[5]	/BG[1]	/HALT[14]
29	/RESET[34]	/BR[1]	/BGACK[1]
30	/IACK[1]	/IRQ	/BERR[14]
31	GND	GND	GND
32	SNDR	GND	SNDL

Note that the data and address bus, as well as most control signals (those in rows 1-25) should be driven through buffers when multiple peripherals are present. These buffers should be direction controlled by the bus request lines, as to allow external bus masters to access CPU board peripherals.

Any empty cells are not currently used and considered reserved for future use, and should be no connect.

Remarks

1. Pulled up on CPU board
2. Pulled down on CPU board
3. Asserted by processor to reset all peripherals. To reset the processor, you must simultaneously assert /RESET and /HALT for at least 1ms.

4. This signal is open drain.
5. Asserted when the currently decoded address is valid *and* is not decoded on the CPU board. Can be used as part of external buffer logic.

Rev1 Assembly Notes

Debug board

- F202 footprint appears to be too large for the fuse ordered (NANOSMDC050F/13.2-2)
4C4B7710-7F08-4D19-BEB5-0A50049FE9E9.jpeg
- F201 is actually 1.1A, not 1.5A as the schematics indicate
- Caps under Teensy (C316/C317) could use with being moved a bit
- U508/U509 package sucks ass
- C512/C511 should be further away from IC in -Y
- The indications for RESET and HALT are inverted (D401, D402) from what they should be
- Teensy USB port interferes with J302 with some USB cables
- Solder pads for DIN connectors could be slightly wider copper
- Logic probe connectors need more spacing in Y direction to fit the probes

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CPU Board

- +12V fuse (F202) footprint is wrong
- Reset and NMI button logic is inverted from what it should be (lol)
  - U501 shouldn't be inverting type (use 74HC2G17 instead)
- D201 should be further set back (.3mm) from board edge
  - The H100 series LED seems to have a slightly different pin-to-front distance than the H201 double LED indicators
- 5V Analog caps (C608, C609, C614) should be up more
- LED current limiting resistors are out of whack
  - Lower the current limiting resistors for right angle LED indicators (needs more current)
  - Increase the current limiting resistors for two bonus debug LEDs (needs less current)
- Read/modify/write cycles may not work right
  - We need to deassert /DTACK when both /LDS and /UDS get deasserted
    - Neither of the byte strobes are on U102, which is responsible for generating /DTACK
    - *May* be able to bodge these into the GAL, since there’s a few spare inputs
  - Also, the /BERR timer and peripheral waitstate generator are reset by /AS
    - Probably a non issue since RAM is going to be 0 waitstate, and we can say CPU board peripherals don’t support read-modify-write (maybe only an issue for NVRAM)
- UART B (J503) should be centered between LEDs and UART A jack